Near Infra-Red Light Detection Using Silicon Avalanche Photodiodes: Design Challenges in Standard CMOS Technology

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BIOGRAPHY

Ehsan Kamrani: Ehsan received his B.Sc. degree in Biomedical engineering from SBMU, Iran, in 2002 and his Masters degree in Electrical and Control Engineering from TMU, Iran, in 2005. He has been with the Institute of Medical Engineering, Salamat-Pajooh-Bartar (05-09), MetaCo. (03-04), Ferdowsray (00,04), Saadat Co. (98-04) and Imen-Ijaz Inc. (99-00) working on design and development of biomedical imaging and real-time monitoring systems. From 2005 to 2009 he has been an Academic Member-Instructor in the Department of Electrical and Electronics Engineering, University of Lorestan, Iran. His expertises are on Analog integrated circuits, smart CMOS image sensors, wireless networked sensors, web-based control systems and biomedical signal/image processing. He published more than 30 papers in peer reviewed journals and conference proceedings. Since 2009 he has been doing his PhD on Biomedical Engineering at Polystim neurotechnologies Laboratory, Ecole Polytechnique, Montreal, Canada. He is working on design and implementation of an fNIRS photo receiver for real-time brain monitoring. From March 2012 he has joined Harvard Medical School and Wellman Center for Photomedicine, Massachusetts General Hospital in Boston, MA, USA working in an active bio-optics project for developing novel innovative technologies by integration of photonics and biological system aiming at developing a novel diagnostic optical instrument for medical applications.

TECHNICAL ABSTRACTS

Silicon-based avalanche photodiodes (SiAPDs) fabricated using highly optimized dedicated processes to achieve excellent device performance can have low doped p and n layer resulting in wide depletion region extending from the cathode to the anode. Due to the availability of wide depletion region, they are efficient for absorption of red and NIR photons. Nevertheless, the SiAPDs fabricated in dedicated process have two major disadvantages: the production cost is very high due to the specialized fabrication process, and it is unfeasible to integrate electronic circuits on the same chip. Later several dedicated SiAPD fabrication technologies were proposed which are compatible with the fabrication of CMOS circuits, and therefore, monolithic integration of APD devices and CMOS circuits became possible. However, optimizing the performance of both the CMOS devices and the SiAPD is a non-trivial job. To overcome these problems, researchers have investigated the design and fabrication of SiAPDs in a standard CMOS process to reduce cost and to maximize miniaturization. The fabrication of SiAPDs in standard CMOS technology permits having both the photodetector and the necessary peripheral circuits on the same chip as an integrated system. However, it is challenging to make SiAPDs in standard CMOS technology due to lack of special fabrication steps. Furthermore, the realization of the APD has to be compatible with the CMOS process characteristics and the APD has to operate with a sufficient voltage, allowing for avalanche mode without destroying the device, particularly at the peripheral junction at the presence of Punch-through, high tunneling, and premature edge breakdown (PEB) effects.

The usually used solution is the implementation of a guard ring that generally consists in a slightly doped region at the peripheral junction because a slightly doped region holds tension better than a heavily doped one. However, even by considering the premature edge breakdown effect and applying different PEB prevention (PEBP) techniques, only a few

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percent of fabricated APDs using standard CMOS technology are functional even with a proper design specifications interpreted from the theory and device simulation results before fabrication.

In this paper we have reviewed the most popular applied techniques for APD fabrication using standard CMOS technology and a new practical and efficient design procedure technique is proposed in order to have a functional fabricated APD, based on our design, simulation and fabrication experiences. The impact of PEB and the most recent progress and techniques for PEBP in CMOS SiAPD design and fabrication are evaluated following by the design, simulation and fabrication of three different proposed guard-ring structures. Inefficiency of the applied PEBP techniques and insufficiency of device simulation results will lead to a low performance or non-functional SiAPD and a significant discrepancy between design simulation and measurement results. In addition to doping profile and electric field distribution in SiAPD structure, the punch-through, high-tunneling and PEB effects should be considered to design a high quality SiAPD using standard CMOS process. The sharpness of the transition between band-to-band tunneling and the avalanche is reported as a critical design criterion.

New APD structures are proposed and implemented using relatively low-doped layers available in standard CMOS process technology. These structures are modified to have a most efficient PEBP to reach maximum efficiency for low-noise and low-intensity light detection in near infra-red wavelength region to be applied in medical imaging applications such as fNIRS. In order to boosts the quality of the APDs, we have to apply a wavelength specific SiAPD design procedure. CMOS SiAPDs with wide depletion region (>10µm) are appropriate for NIR light absorption which necessitates designing the SiAPDs with low-doped layers. The design scales for wavelength specific design, was gained as shown in Fig. 1 and the guard-rings were implemented on p+/n-well red-APD structure. By implementing different APD structures, we have studied the geometric trade-offs involved in the design of deep-submicron APDs. The p-well and p-substrate structures suffer from punch-through, high tunneling and PEB. The APD with n-well based guard-ring structure had highest sensitivity and photon detection probability (PDP) to dark current rate (DCR) ratio characteristics and can be biased properly in Geiger mode. It exhibits a dark count rate of 1 kHz (with 0.5V excess bias at room temperature), a maximum photon detection probability of 70% at maximum excess bias and 9V breakdown voltage.

Keywords: near infra-red photodetection, avalanche photodiode, standard CMOS technology, optimal control, logarithmic transimpedance amplifier, analog integrated circuit, Quench-Reset circuit, photon counting, brain imaging.

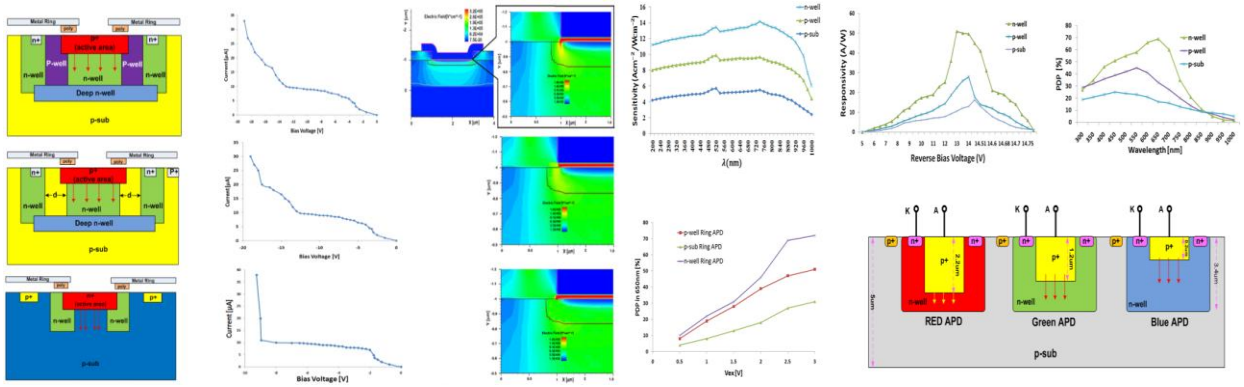


Figure 1. The cross-section, I-V characteristics and the electric field distribution of the p+/n-well and n+/p-sub APDs implemented using standard CMOS technology and Comparison of different implemented CMOS APDs

Optimal-Adaptive Control System for Low-Noise, Low-Power and Fast Photodetection in Functional Near Infra-Red Spectroscopy

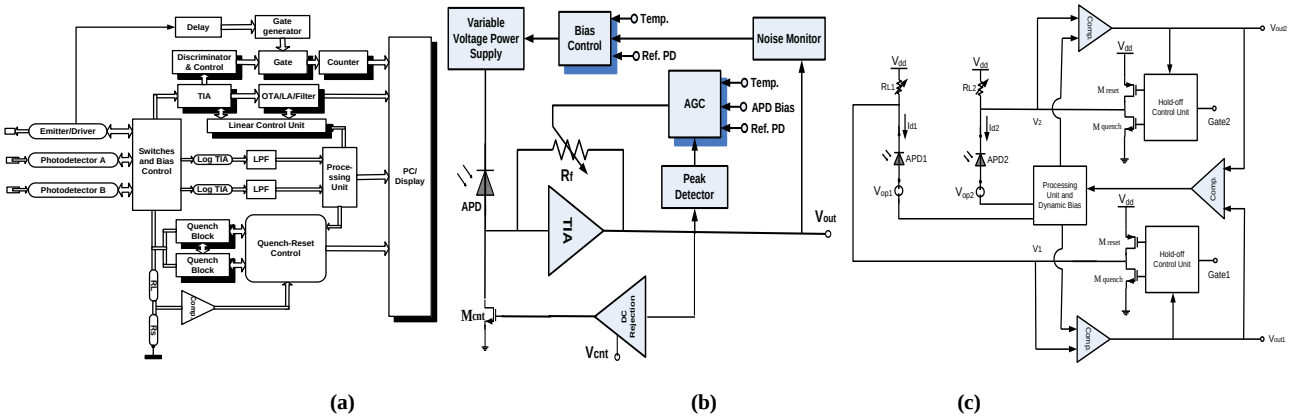
The tradition control systems for photodetection are based on automatic gain, bias or temperature control. These control blocks are off-chip and/or have been designed in order to control over a limited range of temperature or gain variations and require additional circuitry and techniques for providing thermal stabilization for APD to avoid full breakdown of APDs. In traditional TCSPC detectors applied for tomography, using digital circuitry imposes more complexity, higher power-consumption, lower speed and higher cost in to the detector. The image sensor and the photodetection front-end circuitry in common detectors are developed in different packages and are wired off-chip interconnected. Due to the ultra-low intensity of the detected light by image sensor and its sensitivity to the ambient light and peripheral noises these systems suffer from low SNR and high-power consumption.

In order to overcome these limitations, we have designed and developed a miniaturized, reconfigurable, low-noise, and fully-analog integrated NIR light detector. It applies adaptive-optimal control implemented in CMOS technology to achieve a smart imaging sensor for several applications by on-chip detection, amplification, filtering, monitoring, quenching and counting. This system is able to works either as a CW and TCSPC Photodetector on the same platform. The variable and uncontrollable gain of the APD can take it into full avalanche breakdown which can cause catastrophic and irreversible damage to the APD itself. The noise from the APD is also an increasing function of gain so it is desirable to operate the APD such that the gain is just sufficient to bring the shot noise amplified by the avalanche process to the level of the thermal noise of the preamplifier. Furthermore, the background level variation, changes the optimum value of the gain. So maintaining an optimum gain and bias for operating the APD is a critical challenge in designing photodetection system based on APD. We have proposed a new optimal-adaptive integrated control system for on-chip real-time monitoring and automatic control of fNIRS front-end parameters: APD multiplication Gain, Bias, Amplifier Gain and BW, Hold-off time, Ambient light and noise to be applied in a fNIRS photodetection integrated system for real-time brain monitoring. The switch and bias control block, rejects the ambient light, control the bias and emitter power, control the excess bias based on the temperature variation and switched between different modes of operation. The processing unit includes an analog processing circuitry that calculates the ratio, subtract and average of the fNIRS signals from two photodetectors. We used this information in order to calculate the avalanche gain, noise effects and ambient light, dark current rate, and remove the superficial signals effects. Using this technique, the signal originating from the proximal receptors is subtracted from the distal ones, therefore only information from the deeper part of the brain is displayed.

This system has the ability to real-time optimal-adaptive control of avalanche gain, avalanche bias, temperature, light-power, light duration, detection efficiency, depth and spatial resolution, amplification gain and BW, ambient light and dark current, quench-reset speed, hold-off time and detection timing all included in a single on-chip detector system. In order to keep the APD gain stable under temperature variations we develop an automatic gain monitoring and control (AGC) mechanism on our proposed TIA circuit that also increase the input dynamic range. We have also implemented an automatic-adaptive bias control (ABC) system for closed-loop adaptive-optimal control of the APD biasing over varying operating conditions such as temperature or ambient illumination and changes in photodiode parameters. We use an adaptive power supply to determining an optimum bias voltage for the APD. This circuit measures the output noise level of the APD, and generates a control signal that feeds to a variable voltage power supply. This mechanism also controls the noise and eliminates the requirement for thermal stabilization circuitry associated with APDs so optimizes the operation of the APD and the whole photoreceiver front-end either. In order to improve the intelligence of the control system, a theoretical model of temperature and noise compensation can be implemented in the control block for APD biasing. By implementing different SPAD structures, we studied the geometric trade-offs involved in the design of deep-submicron APDs. We studied the wavelength dependency of the different APDs and the optimal scales for NIR-sensitive APD design are selected. Based on our results, the p-well and p-substrate structures suffer from punch-through, high tunneling and PEB. The APD with n-well based guard-ring structure had highest sensitivity and PDP to DCR ratio characteristics and could be biased properly in Geiger mode. It exhibits a dark count rate of 1 kHz (with 0.5V excess bias at room temperature), a maximum photon detection probability of 70% at maximum excess bias and 9V breakdown voltage.

Using the number of the photons in the light pulse, we reduces the time walk effect by applying a correction lookup table. The photon number determination is performed with a linear-mode APD connected to an analog to digital converter. The photo number measured by the linear photodetector can only give an evaluation of the photon number impinging the Geiger photo detector. Then, due to the time walk of the Geiger detector, this photo number uncertainty

introduces a time uncertainty that has to be considered especially in low number photon condition. Here we simultaneously bias the dual input APDs in different modes of operation and measure this uncertainty without using any extra circuitry. We developed a new on-chip signal processing unit for automatic control and tuning of the hold-off time of the SPAD. This circuit eliminates after-pulsing effects in a GM-APD using dual APD data and autocorrelation statistics. We use a new multi-model adaptive-optimal control system which smartly selects the optimal hold-off time in a MQRC. This circuit optimizes the hold-off time to reduce after-pulsing effects in GM-APD. An optimal control blocks in this technique automatically selects the optimal hold-off time value corresponding to the minimization of after-pulse effects in the GM-APD. The proposed TIA has a very low power consumption (135µW), high transimpedance gain (up to 300MV/A), tunable BW (1KHz-1GHz) and very low input and output noise (<10fA/√Hz and 0.5µV/√Hz). The proposed system has been designed and developed in Virtuoso Cadence environment and its optical and electrical characteristics has been verified using Matlab, Comsol and TCAD device simulators. This design has been scheduled to be fabricated in CMOS 0.18µm technology in TSMC via CMC and the experimental in-vivo measurement results will be reported after device shipment.



(a) **(b)** **(c)**

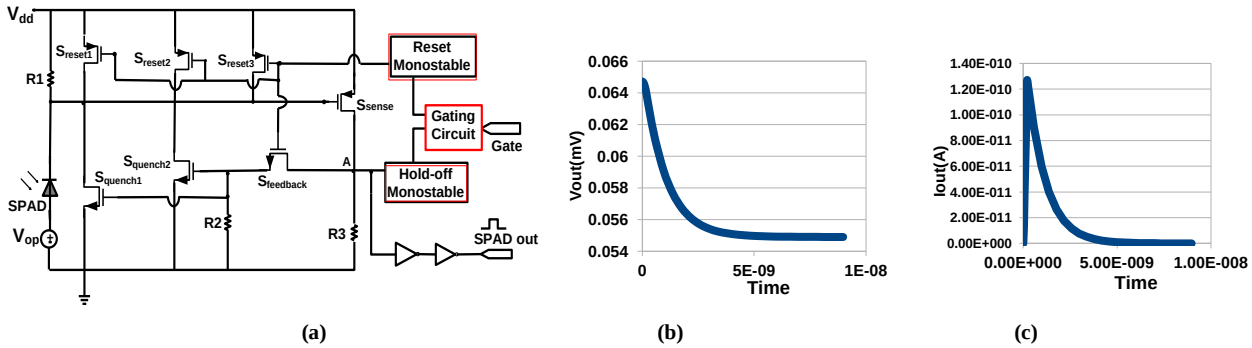
Fig. 2: Block-diagram of the proposed fNIRS front-end (a), the Schematic diagram of the proposed controlled mixed quenching circuit with dual APD detector technique (b) and the on-chip signal processing unit for automatic control and tuning of the hold-off and the proposed TIA with AGC, ABC and ambient light rejection loops (c)

Fast Photodetection in Functional Near Infra-Red Spectroscopy

In order to operate the single photon avalanche photodiode (SAPD) in Geiger mode for single photon counting, a new controllable mixed quenched circuit (MQC) with ability to real-time control of hold-off time in photoreceptor front-end is proposed in this paper. It exhibits an ultra-fast quench time (<1ns) with a low power consumption (4mW) and less complexity accompanying with more flexibility and dynamic range of operation by developing an adaptive and fast hold-off time control on the available traditional quench circuits. Due to the complementary action of the active quench circuit (AQC) in MQC in order to suppress more the initially quenched avalanche by the passive quench circuit (PQC), there is more flexibility in choosing the PQ load (RL). Therefore by reducing the load resistor RL one can achieve a quicker detection of the photon. By increasing the light intensity received by the APD, the current flow through the diode and the series connected resistor (RL) will also increase. The resulting increase voltage drop across the RL, decreases the bias voltage across the APD, so that the gain of the APD is reduced. Therefore the dynamic range of optical input of the APD will be increased for a fixed dynamic range of electrical output. Using this circuit, faster quenching results in lower power loss and hence less heating of the SPAD.

Because in fNIRS systems usually several detectors are applied, designing the detection system based on dual (and multi) detector topology helps to design a more compact, reliable and precise detector and reduces the cross-talk and mismatch interferences which are important challenges of traditional separate photodetectors. Here we use the current-

mode PQC at the first stage which increases the detection rate comparing to the voltage-mode PQC circuit with longer pulses. The proposed Dual SPAD Quench-Reset (DSQR) technique provides a collaborative between two SPADs in order to quench and reset each other consequently. We can reach zero hold-off time SPADs and considering one quench-reset circuit for several simultaneously activated APDs in an array of APD systems is also possible using this technique.



(a) **(b)** **(c)**

Figure 3. Schematic diagram of the proposed controlled mixed quenching circuit (a) and the APD cathode Voltage (b) and current (c) in response to single Photon Arrival

State-of-the-Art Logarithmic Transimpedance Amplifier With Automatic Gain Control and Ambient Light Rejection for fNIRS

Logarithmic transimpedance amplifier (LogTIA) is practically useful in systems that need scale-invariant and wide dynamic range operation. Its sensitivity to the contrast (ac/dc) of the input and its scale-invariant fractional amplification is beneficial in several applications where percentage changes rather than absolute changes carry information. This photoreceptor was inspired by the operation of biological photoreceptors in turtle cones and bears many of its properties including higher ac gain than dc gain, a contrast-sensitive response, and a relatively wide dynamic range of operation. Unfortunately, the merit characteristics of this amplifier specially for biomedical imaging and optoelectronics circuits and systems are not introduced well and only a limited application of LogTIA in photodetectors implementation are reported. In this paper we have introduced the unique characteristics of LogTIA as a state-of-the-art front-end circuit for photodetection especially in near infra-red region of light spectrum. Here we have designed and implemented a new LogTIA to be applied in functional near infra-red spectroscopy (fNIRS) photodetector front end. This is the first proposed and successfully designed and implemented application of LogTIA in a near infra-red photodetector front-end and in fNIRS application.

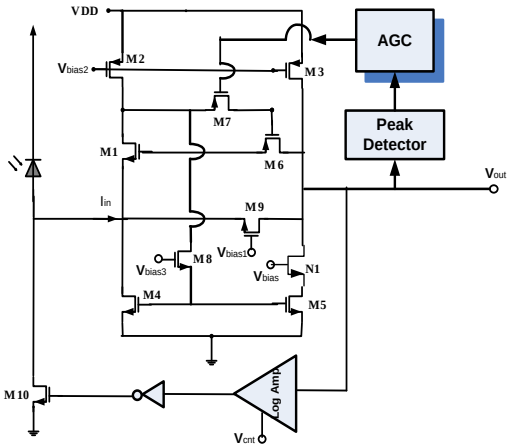
In this circuit (Fig. 4), M1 act as the logarithmic amplifier transistor, M6-M7 provides the feedback resistor. M9 acts as a feedback transistor placed directly across the input and output terminals of the current mirror. Using this direct feedback topology, decrease the input impedance seen by the photodiode and improve the speed of the circuit by the cost of the lower output swing. Using logarithmic amplifier makes also the response to a fixed image contrast invariant to absolute light intensity and improves the dynamic range of the photodetector. The N1 transistor at the output of TIA, cause the circuit acts as a cascade current mirror, reduce the output voltage variation by boosting the output impedance and reduce the v_{DS} -mismatch effect. Using an automatic gain control and DC rejection feedback we have increased the sensitivity and BW. The transimpedance gain of the linear TIA increases the sensing speed by decreasing the time constant such that the rapid changes in the input are not filtered at the output. The input voltage (V_{in}) is kept at a virtual reference value (V_{ref}) by the feedback loop such hat it doesn't change by the variation of the input current, thus the current variations due to the Vin variation (e.g. due to early effects and other sensor effects), are minimized. By increasing the power supply, the dynamic range of the output voltage can be maximized while maintaining the avalanche photodiode (APD) breakdown voltage at the input. In contrast, the logarithmic TIA shown in Fig. 4, uses a sub-threshold

transistor as the feedback element with an exponential parameter of κ_s (the sub-threshold exponential coefficient of M_f) and a pre-exponential constant of I_{os}. The key motivation for using the logarithmic instead of linear sensing is that it is inherently sensitive to the contrast (ac/dc) of the input photocurrent signal. By assuming V_{ref} and considering that the i_{in} and v_{out} are the small changes in the operating-point current (I_{IN}) and voltage (V_{out}) respectively, the output voltage of the LogTIA is equal to:

$$v_{out}(s) = \frac{KT}{q}\left(\frac{i_{in}}{I_{IN}}\right)\left(\frac{A/(1+A)}{1+\frac{s(C_{in}/g_f)}{1+A}}\right) = \frac{KT}{q}\left(\frac{\Delta I_{IN}}{I_{IN}}\right)\left(\frac{A/(1+A)}{1+\frac{s(C_{in}/g_f)}{1+A}}\right) = V_{ref} + \frac{KT}{q\kappa_s} ln\left(\frac{I_{in}}{I_{Ios}}\right)$$

$$v_{out} = \left(\frac{dV_{out}}{dI_{in}}\right) i_{in} = \left(\frac{KT}{q\kappa_s} \times \frac{1/I_{Ios}}{I_{in}/I_{Ios}}\right) i_{in} = \left(\frac{KT}{q\kappa_s}\right) \times \left(\frac{i_{in}}{I_{in}}\right) = \left(\frac{KT}{q\kappa_s}\right) \times \left(\frac{i_{ac,in}}{I_{DC,in}}\right)$$

So in LogTIA, the output voltage is proportional to the ac/dc of the input current as expected. It converts the small fractional changes in input ($\frac{\Delta I_{IN}}{I_{IN}}$) into an output voltage while increasing the speed of the input time constant by the factor of (1+A). Contras to the linear TIA, The time constant of LogTIA depends on the operating point and varies linearly with I_{IN} (g_f depends on I_{IN}). The LogTIA provides a wide dynamic range operation with a moderate power supply voltage. The minimum detectable contrast in a LogTIA is not depends on the input current intensity because the BW and therefore integration interval of the system scales with input current so that a constant number of the electrons is always gathered during the sensing period. In linear TIA, the BW and subsequently the integration intervals of the system are fixed such that the minimum detectable contrast is worsened at low input intensities due to the gathering of the more electrons. The LogTIA can be considered as a linear TIA with a built-in gain controller, such that the feedback resistance (R_f) varies with I_{in} to keep the $I_{in}R_f$ fixed. In order to keep the photodetector gain stable under temperature and ambient light variations we develop an automatic gain monitoring and control (AGC) mechanism and an ambient light rejection circuit (include Log Amp, buffer and M10) on our proposed TIA circuit that also increase the input dynamic range.



Parameter	Value	
	LogTIA	LogTIA+AGC and Noise Rejection
Fabrication technology	CMOS 0.18µm	CMOS 0.18µm
Supply voltage (V)	1.8	1.8
Max. Swing (V)	1.8	1.8
Max Gain	220 M	300 M
Power diss. (mW)	0.04	0.5
BW (MHz)	0.1-1000	0.001-5000
Input Noise at 1kHz (A/√Hz)	100 f	< 10 f
GBW/Power dis. (GHzΩ/mW)	5.5 M	3 G
Sensitivity (dBm)	-32	-42
Data rate (Gb/s)	3.04	3.4
Bit Error Rate (BER)	10^{-11}	10^{-13}
PRBS	$2^{31}-1$	$2^{33}-1$

Figure 4. Proposed logarithmic TIA with ambient light rejection and AGC loops (left), and its characteristics (right)